AMENDMENTS TO THE SPECIFICATION

Page 4, paragraph beginning on line 12, spanning pages 4 and 5, delete in its entirety, and replace with the following:

In ~~jet~~ yet another aspect of the invention, the object is achieved by a master program module for a (first) module having a first clock generator for synchronization with at least one second module having a second clock generator, wherein the master program module contains a program code that can be run by a control means of the first module, the master program module further comprising

- transmitting means for sending a first clock signal generated by the first clock generator to the at least one second module,
- receiving means for receiving at least one second clock signal generated by the second clock generator that is synchronized with the first clock signal and sent by the at least one second module, and
- generating means for forming a (first) time difference value between first clock signal and the at least one second clock signal, which time difference value is essentially due to the transmission time of the first and of the at least one second clock generator between the first, and the at least one second module,

wherein the transmitting means are designed for sending an item of information about the (first) time difference value to the at least one second module.

Page 5, second full paragraph, delete in its entirety, and replace with the following:

In ~~jet~~ yet another aspect of the invention, the object is achieved by a slave program module for a (second) module having a clock generator for synchronization with at least one first module, wherein the slave program module contains a program code that can be run by a control means of the second module, the slave program module further comprising

- receiving means for receiving a first clock signal sent by the first module,
- synchronizing means for synchronizing the clock generator on the basis of the first clock signal, and
- transmitting means for sending a second clock signal synchronized with the first clock signal to the first module,

wherein the receiving means are designed to receive an item of information transmitted by the first module about a (first) time difference value formed from the first clock signal and the second clock signal, which time difference value is essentially due to the transmission time of the first and of the at least one second clock signal between the first, and the at least one second module, and wherein the synchronizing means are designed to adjust the clock generator on the basis of the information about the (first) time difference value.

Page 5, second paragraph, spanning pages 5 and 6, delete in its entirety, and replace with the following:

In ~~jet~~ yet another aspect of the invention, the object is achieved by a device, in particular a telecommunication device, containing at least one first and at least one second module, each having a clock generator, wherein the at least one first module comprises

- transmitting means for transmitting a first clock signal generated by the first clock generator to the at least one second module.
- receiving means for receiving at least one second clock signal generated by the respective second clock generator and synchronized with the first clock signal and transmitted by the at least one second module, and
- generating means for forming a (first) time difference value between the first clock signal and the at least one second clock signal, which time difference value is essentially due to the transmission time of the first and of the at least one second clock signal between the first and the at least one second module,

wherein the transmitting means are designed for sending an item of information about the (first) time difference value to the at least one second module and wherein the at least one second module comprises

- receiving means for receiving a first clock signal sent by the first module,
- synchronizing means for synchronizing its clock generator on the basis of the first clock signal, and

- transmitting means for sending a second clock signal synchronized with the first clock signal to the first module,

wherein the receiving means are designed for receiving an item of information sent by the first module about a (first) time difference value formed from the first clock signal and the second clock signal, which time difference value is essentially due to the transmission time of the first and of the at least one second clock signal between the first and the at least one second module, and wherein the synchronizing means are designed for adjusting the clock generator on the basis of the information about the (first) time difference value.

Page 11, first full paragraph, delete in its entirety, and replace with the following:

The module MOD2 transmits the clock signal TS2DEL to the module MOD1. Transmission time is likewise needed for this purpose. The module MOD1 determines a time difference value DIF1 between the clock signal TS1 and the clock signal TS2DEL it receives. The time difference value DIF1 is essentially due to the transmission time of the clock signal TS1 from the module MOD1 to the module MOD2 and the transmission time of the clock signal TS2DEL from the module MOD2 to the module MOD1. Since the transmission paths between the modules MOD1 and MOD2 are equally long in the present case, the logic component CP1 halves the time difference value DIF1 and forms an item of correction information COR. The module MOD1 then transmits the correction information ~~CORto~~ COR to the module MOD2, which adjusts its clock generator GEN2 with the correction information COR. The clock generator GEN2 then generates a clock signal TS2OPT that is synchronous with the clock signal

TS1. If the transmission paths between the modules MOD1 and MOD2 are not equally long, the logic component CP1 may also use other, more complex algorithms to form the correction value COR1.

Page 11, second full paragraph, delete in its entirety, and replace with the following:

The correction information ~~CORmay~~ COR may contain, for example, a digitally encoded transmitted starting value or a resettable counter contained in the clock generator GEN2. It is also possible that the module MOD1 corrects the clock signal TS1 forward in phase by the halved time difference value DIF1 between the clock signal TS1 and the clock signal TS2DEL and transmits the clock signal TS1 "advanced" in this way as correction information ~~CORto~~ COR to the module MOD2.

Page 12, first full paragraph, delete in its entirety, and replace with the following:

Furthermore, the module MOD1 may transmit the time difference value DIF1 between the clock signal TS1 and the clock signal TS2DEL also in unprocessed form, that is to say as correction information ~~CORto~~ COR to the module MOD2 without the halving described above. The module MOD2 then halves the time difference value DIF1 and thus adjusts its clock generator GEN2. Furthermore, the module MOD2 may incorporate, for example, also an offset value in the correction information COR. Such an offset value may represent, for example, the time that the clock generator GEN2 requires for the adjustment operation or that the module MOD2 needs to receive and read in the correction value COR1.

Page 12, second full paragraph, delete in its entirety, and replace with the following:

Let the sequence shown in Figure 2 be preceded by the synchronization shown on the basis of Figure 1. The clock generators GEN1 and GEN2 generate clock signals TS1 and TS2, respectively, that are synchronous under optimum conditions, for example in the case of interference-free clock generators GEN1 and GEN2 operating in exactly the same way. The module MOD1 transmits the clock signal TS1 to the logic component CP2 of the module MOD2. Furthermore, the logic component CP2 receives the clock signal TS2 from the clock generator GEN2. From the clock signal ~~TS1~~ TS1, delayed by the transmission from the module ~~MOD1~~ MOD1, and the local clock signal TS2, the logic component CP2 forms a time difference value DIF2 that, given synchronous clock signals TS1 and TS2, ~~are~~ is equal to half the time difference value DIF1.

Page 15, first full paragraph, delete in its entirety, and replace with the following:

The module MOD2 transmits the clock signal TS2 with the aid of its transmitting module SND21 on a bus line BUSRCV for the module MOD1, which receives the clock signal TS2 with the aid of a receiving module RCV11. The logic component CP1 forms the correction information ~~CORin~~ COR in a manner known from Figure 1 and transmits it with the aid of a transmission module SND12 on a bus line CORX to the module MOD2. The latter receives the correction information ~~CORwith~~ COR with the aid of a receiving module RCV22 and adjusts its clock generator ~~GEN2~~GEN2.

Page 15, third full paragraph, delete in its entirety, and replace with the following:

The receiving module RCV22 of the module MOD2 passes on the correction information ~~CORalso~~ COR also to the logic component CP2 so that the latter can, as explained on the basis of Figure 2, generate, on the one hand, the correction value COR2 for the clock generator GEN2 for the purpose of adjusting it and, on the other hand, the time difference value DIF2 that a transmitting module SND22 sends on a bus line DIFX to the module MOD1.